



Aalborg Universitet

AALBORG UNIVERSITY  
DENMARK

## Impact of the Case Temperature on the Reliability of SiC MOSFETs Under Repetitive Short Circuit Tests

Du, He; Reigosa, Paula Diaz; Iannuzzo, Francesco; Ceccarelli, Lorenzo

*Published in:*

34th Annual IEEE Applied Power Electronics Conference and Exposition, APEC 2019

*DOI (link to publication from Publisher):*

[10.1109/APEC.2019.8722300](https://doi.org/10.1109/APEC.2019.8722300)

*Publication date:*

2019

*Document Version*

Accepted author manuscript, peer reviewed version

[Link to publication from Aalborg University](#)

*Citation for published version (APA):*

Du, H., Reigosa, P. D., Iannuzzo, F., & Ceccarelli, L. (2019). Impact of the Case Temperature on the Reliability of SiC MOSFETs Under Repetitive Short Circuit Tests. In *34th Annual IEEE Applied Power Electronics Conference and Exposition, APEC 2019* (pp. 332-337). [8722300] IEEE Press. I E E Applied Power Electronics Conference and Exposition. Conference Proceedings <https://doi.org/10.1109/APEC.2019.8722300>

### General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal -

### Take down policy

If you believe that this document breaches copyright please contact us at [vbn@aub.aau.dk](mailto:vbn@aub.aau.dk) providing details, and we will remove access to the work immediately and investigate your claim.

# Impact of the Case Temperature on the Reliability of SiC MOSFETs under Repetitive Short Circuit Tests

He Du, Paula Diaz Reigosa, Francesco Iannuzzo, Lorenzo Ceccarelli  
Center of Reliable Power Electronics (CORPE)  
Department of Energy Technology, Aalborg University  
Aalborg 9220, Denmark  
hdu@et.aau.dk, pdr@et.aau.dk, fia@et.aau.dk, lce@et.aau.dk

**Abstract**—In this paper, the reliability of SiC MOSFETs under repetitive short-circuit conditions is investigated. At first, the maximum short-circuit withstanding time is studied at three different case temperatures and the critical energy is identified in each case. Thereafter, the repetitive short-circuit tests are performed with fixed pulse time duration and bias voltage. The increasing gate leakage current measured at the interval of repetitive short-circuit tests is observed and the gate oxide failure is confirmed. Then, the results of repetitive short-circuit tests with respect to different case temperatures are presented, which helps to find a correlation between the number of repetitions to failure and the initial case temperature. The impact of repetitive short-circuit tests on the bond wire resistance is also analyzed.

**Keywords**—Silicon carbide, power MOSFET, short-circuit test, case temperature

## I. INTRODUCTION

In recent years, Silicon Carbide (SiC) power semiconductor devices are becoming more and more attractive in power electronics applications thanks to their superior physical properties over silicon, such as breakdown electric field, thermal conductivity, bandgap energy and carrier velocity, which provide the capability for high switching, high voltage and high temperature operations [1]. SiC MOSFETs with the voltage of 1.2 kV and 1.7 kV have been widely commercialized, and the 3.3 kV [2], 6.5 kV [3] and even higher [4] [5] power devices have been proposed.

However, the reliability of SiC MOSFETs has not been fully understood especially under abnormal operating conditions, such as overcurrent, overvoltage, Unclamped Inductive Switching (UIS) [6] and Short Circuit (SC) [7]. Among these, the SC conditions receive extensive attention due to both high current and voltage, which is crucial to the reliability and failure protection [8].

So far, two chip-related failure mechanisms under SC conditions have been discussed in [9]. Thermal instability is one of the weaknesses; during single SC event, the high energy is dissipated in a relatively short time and the internal temperature increases. The drain leakage current, caused by the drift of thermally generated carriers, could trigger a positive temperature feedback when it achieve at considerable value and eventually lead to the thermal runaway [10].

The other failure mechanism is the gate damage. The gate oxide thickness need to be thinner due to the low electron mobility of SiC material and therefore the gate structure is the fragile part [11]. The leakage current from gate to source, generated by the reach-through phenomenon, would be increased by the high electric field and high temperature [8].

In [12], four different resistive paths have been observed. Furthermore, SC conditions could also cause a package-related degradation at the interface between the bonding wires and dies as well as the solder interface layer [12].

With the aid of repetitive SC tests, the aging indicators can be explored comprehensively. The shift of gate threshold voltage, increase of gate leakage current, drain leakage current and on-state resistance [8] [13] [14] have been proposed to evaluate the degradation after repetitive SC events. In addition, the effect of temperature needs to be considered in the operating conditions or real-application scenarios. In [15], the temperature-dependent SC characteristics and capability are summarized, combined with failure analysis at the case temperature of 25 °C and 200 °C. However, the impact of case temperature on the reliability still need to be investigated.

In this paper, the reliability of 1000 V/ 22 A discrete SiC MOSFETs with planar technology is presented under SC conditions. This work mainly focuses on the influence of case temperature under repetitive SC tests. Electrical parameters are monitored during the tests and the gate-source voltage, which is related to the gate leakage current, is used as the aging indicator. The maximum SC time duration with respect to case temperature is evaluated at first and then a correlation between the number of SC repetitions ( $N_{SC}$ ) and case temperatures is presented.

The remainder of paper is organized as follows. In Section II, the SC test setup for SiC MOSFETs are presented and the maximum SC withstanding time at different case temperature are summarized. In Section III, the relationship between gate-source voltage during SC tests and the gate leakage current measured by static characterizations are verified. The results of repetitive SC tests with respect to different case temperatures and discussion are demonstrated. Meanwhile, the impact of repetitive SC tests on the bond wire resistance is also presented. Section IV gives the conclusions.

## II. MAXIMUM SHORT-CIRCUIT TIME WITH RESPECT TO CASE TEMPERATURE

### A. Configuration of Experimental Setup

A 2.4 kV/ 10 kA Non-Destructive Tester (NDT) has been used for SC tests. The principle schematic of SC test and its appearance are shown in Fig. 1 and Fig. 2, respectively. The high-voltage capacitor bank  $C_{DC}$ , which is charged up by a high voltage power supply  $V_{DC}$ , provides the needed energy for SC test. The series protection, consisting of 4 paralleled IGBT power modules, would be switched off immediately after the SC in order to prevent explosions and allow failure

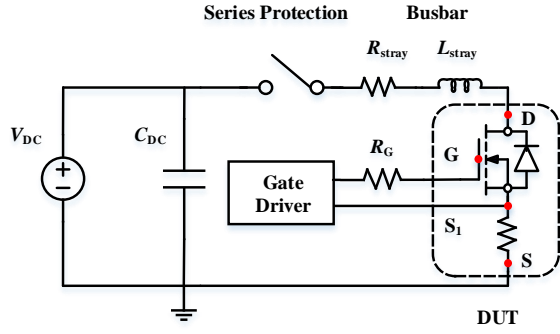


Fig. 1. Principle schematic of the Non-Destructive Tester (NDT).

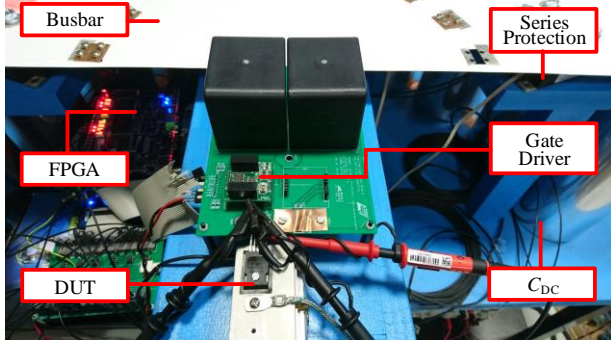


Fig. 2. Appearance of NDT with DUT and PCB adaptor.

analysis. The busbar is well designed with low stray

inductance (10 nH) and a 100 MHz FPGA provides the control signals to the gate drivers for both series protection and Device Under Test (DUT). The DUT is driven by a +15 V/-4 V gate voltage and the used gate resistance is equal to 6.7  $\Omega$ . During the SC tests, drain-source voltage, drain current and gate-source voltage waveforms are measured by the HDO6054-MS oscilloscope.

The DUT is a 1.0 kV/ 22A discrete SiC MOSFET with 3<sup>rd</sup> generation planar technology and it has low source inductance package with separate driver source pin (TO-247-4). Different case temperatures of DUT are achieved by a temperature controller and electrical heater. The thermal conductivity of the Thermal Interface Material (TIM) is equal to 2.5 W/m·K.

### B. Temperature-Dependent Maximum SC Withstanding Time

The maximum SC withstanding time is experimentally investigated at different case temperatures. The results help to identify the critical energy and make sure that the selected testing conditions for the repetitive SC tests are below the critical SC energy.

Fig. 3 shows the SC waveforms under a bias voltage of 600 V with increasing pulse time duration at three case temperatures (i.e.  $T_C = 25^\circ\text{C}$ ,  $100^\circ\text{C}$  and  $150^\circ\text{C}$ ). It can be observed that a tail current appears at turn-off for SC pulse durations larger than 2.5  $\mu\text{s}$ . This phenomena is in agreement with previous work [9] and its mechanism is also confirmed in [10] and [14]. The high temperature within the depletion region could increase the intrinsic carrier density fast and

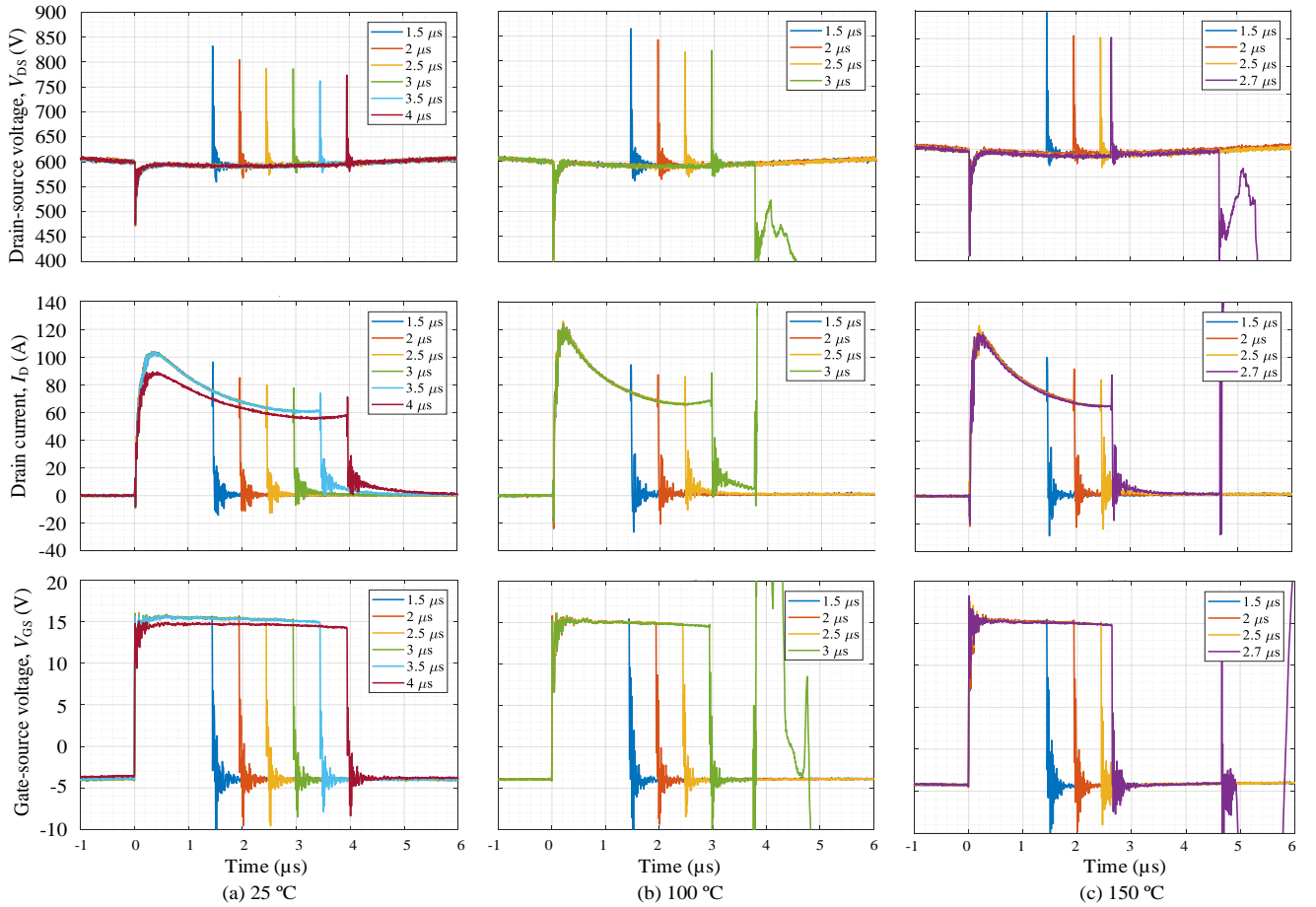


Fig. 3. Drain-source voltage, drain current and gate-source voltage waveform of SC tests with increasing time duration at different case temperatures.

lead to a thermal generation current, which dominates the total leakage current. If the leakage current is high enough, thermal runaway would happen [15]. In Fig. 3 (b) and (c), the devices fail after turn off, which confirms the thermal runaway mechanism. The SC withstand time duration decreases from 4  $\mu\text{s}$  to 3  $\mu\text{s}$  and then 2.7  $\mu\text{s}$  when the initial case temperature increases from 25  $^{\circ}\text{C}$  to 100  $^{\circ}\text{C}$  and 150  $^{\circ}\text{C}$ . The SC energy is calculated when the failure is observed, being 0.15 J, 0.13 J to 0.12 J with increasing case temperature.

### III. REPETITIVE SHORT-CIRCUIT TESTS

#### A. Aging Indicators

In order to evaluate the impact of the initial case temperature on the number of SC repetitions, the aging indicators are firstly investigated. The static characteristics of DUT are measured before repetitive SC tests by the Power Device Analyzer B1506A.

With the aim of performing the repetitive SC tests below the maximum SC critical energy, the test conditions are set to  $V_{\text{DC}} = 600 \text{ V}$ ,  $t_{\text{SC}} = 2.2 \mu\text{s}$  and  $T_{\text{C}} = 25 ^{\circ}\text{C}$ . Initially, the static characteristics, including threshold voltage ( $V_{\text{th}}$ ), gate leakage current ( $I_{\text{GSS}}$ ), drain leakage current ( $I_{\text{DSS}}$ ) and on-state resistance ( $R_{\text{DS,on}}$ ) are measured before the first SC test. Then, the repetitive SC tests are performed, and the drain-source voltage ( $V_{\text{DS}}$ ), gate-source voltage ( $V_{\text{GS}}$ ) and drain current ( $I_{\text{D}}$ ) waveforms are recorded. After each 10 SC repetitions, the static characterization is performed again.

The drain current and gate voltage waveforms of repetitive SC tests from the 20<sup>th</sup> to 140<sup>th</sup> repetition are shown in Fig. 4. The reduction of the on-state gate-source voltage and therefore on-state drain current are observed with increasing number of repetitions. This phenomenon is related to the gate oxide degradation.

In the case of static characterization, the gate leakage current increases with the applied gate bias increase. When the  $V_{\text{GS}}$  is equal to 15 V, the gate leakage current reaches its maximum value, which can reflect the gate degradation level. An obvious correlation between the on-state gate voltage during SC tests and the gate leakage current measured by static characterization is obtained. Fig. 5 shows the reduction of on-state gate voltage at 2  $\mu\text{s}$  and the increase of gate leakage current with the number of SC repetitions increasing. The SC tests are stopped at 140<sup>th</sup> repetition when the maximum gate leakage current achieves at 100 mA and in this case, the minimum gate voltage at 2  $\mu\text{s}$  is equal to 13.6 V, which is decreased by 9.3% comparing to 15 V. Therefore, the on-state gate voltage at 2  $\mu\text{s}$  during SC tests (nearly at the end of the pulse time duration) is selected as the aging indicator and used in the following tests.

#### B. Repetitive SC Tests at Different Temperatures

The repetitive SC tests are performed with 600 V bias voltage and 2.2  $\mu\text{s}$  pulse time duration at 25  $^{\circ}\text{C}$ , 100  $^{\circ}\text{C}$  and 150  $^{\circ}\text{C}$ , respectively. Fig. 6 presents the drain voltage, drain current and gate voltage waveforms at different temperatures and the gate oxide degradation similar to Fig. 4 is observed in each case; the on-state gate voltage and drain current decreases with the number of SC repetitions increasing.

According to the correlation in Fig. 5, when the on-state gate voltage at 2  $\mu\text{s}$  is smaller than 13.6 V, the device could

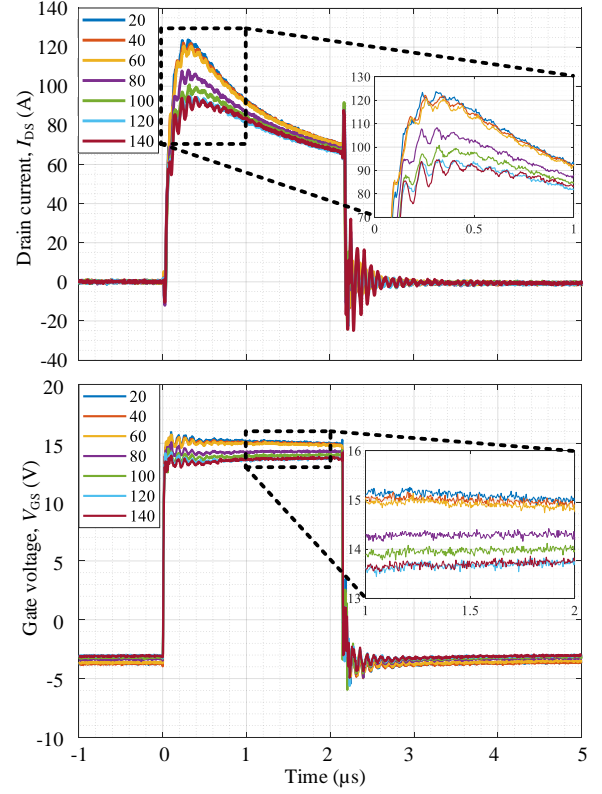


Fig. 4. Drain current and gate voltage waveforms of repetitive SC testd from 20<sup>th</sup> to 140<sup>th</sup> repetition at 25  $^{\circ}\text{C}$  case temperature.

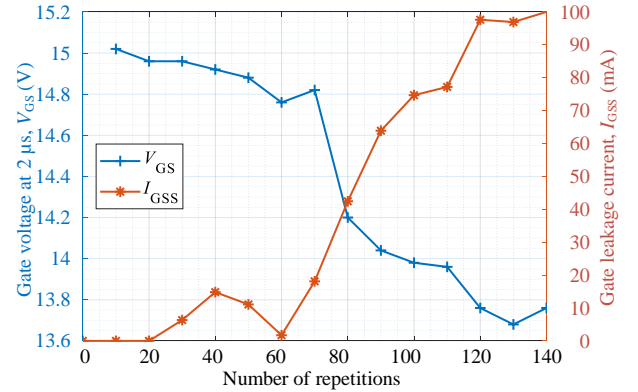


Fig. 5. Correlation between the on-state gate voltage ( $t = 2 \mu\text{s}$ ) and gate leakage current ( $V_{\text{GS}} = 15 \text{ V}$ ).

be considered as failed device. The  $V_{\text{GS}}$  variation with increasing repetitions at 25  $^{\circ}\text{C}$ , 100  $^{\circ}\text{C}$  and 150  $^{\circ}\text{C}$  are shown in Fig. 7. Therefore, the number of repetitive SC tests until failure,  $N_{\text{SC}}$ , could be obtained and it increases from 194 repetitions (25  $^{\circ}\text{C}$ ) to 224 repetitions (100  $^{\circ}\text{C}$ ) and then 422 repetitions (150  $^{\circ}\text{C}$ ) with the case temperature increase. The correlation between number of repetitions and initial case temperature is presented in Fig. 8.

One may think that the increasing case temperature could lead to early failures; however, this is not the case for SiC MOSFETs since the drain current peak decreases with temperature due to its negative temperature coefficient, leading to lower SC energies. During a SC transient, the junction temperature rises faster in terms of lower case temperature and the higher current density would lead to a

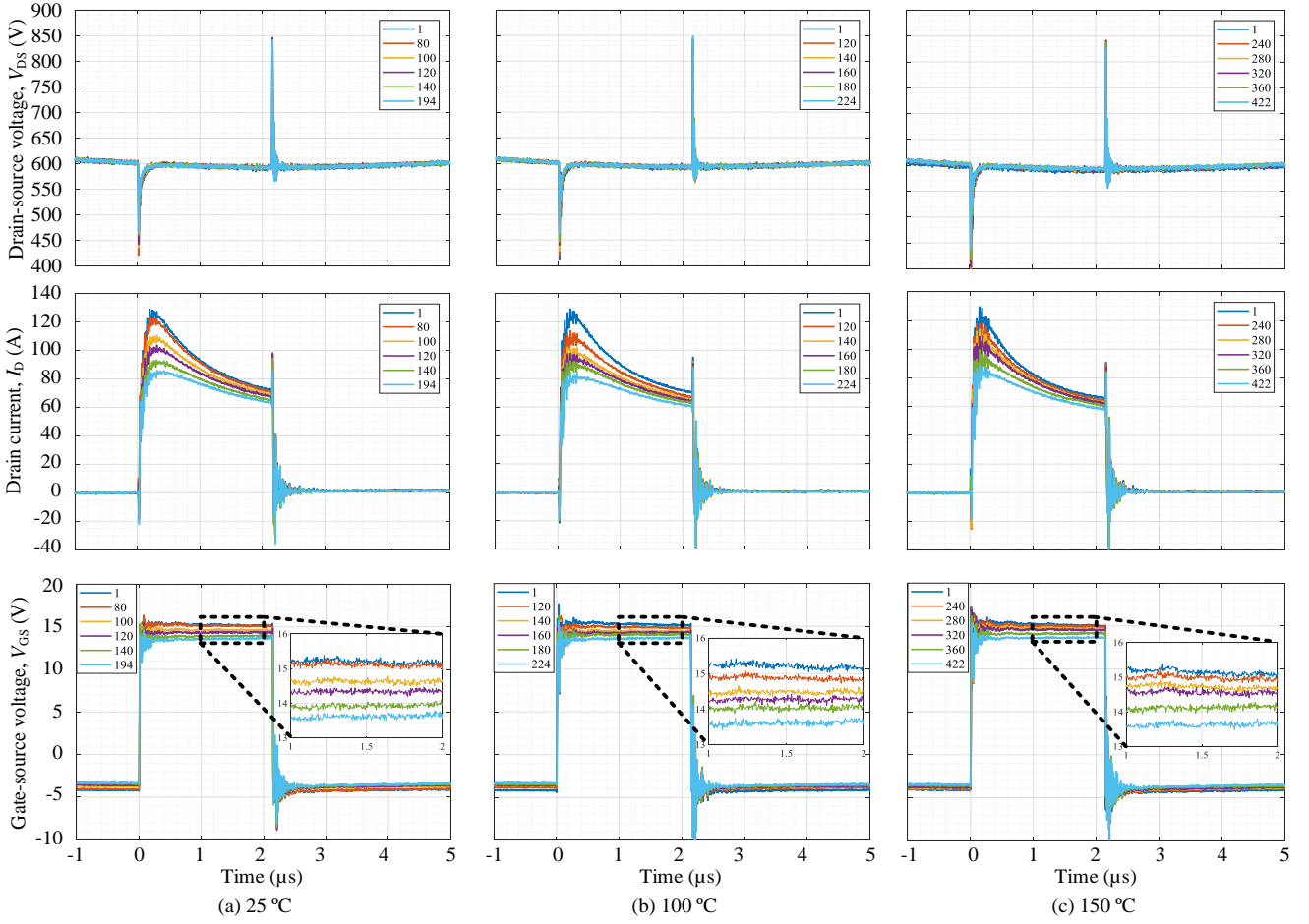


Fig. 6. Drain-source voltage, drain current and gate-source voltage waveform of repetitive SC tests with fixed pulse time duration ( $t = 2.2 \mu s$ ) at different case temperatures.

larger temperature gradient and thus larger number of repetitions.

As can be seen in Fig. 9, the drain current peak during the first SC test at 150 °C case temperature is the lowest one and the drain current peak at 25 °C is higher than 100 °C. The SC energy from  $t = 0$  to  $2.2 \mu s$  are also calculated for the repetitive SC tests with respect to different case temperatures, as shown in Fig. 10. In the beginning stage (SC tests within 100 repetitions), the SC energy in terms of the case temperatures agrees with the hypothesis mentioned above and all of them below 0.12 J, which is the critical energy at 150 °C. Thereafter, when more than 100 repetitions are performed, the SC energy reductions are mainly dominated by the reduced drain current caused by gate degradation.

### C. The impact on bond wire resistance

During the tests, the voltage drop across the bond wire ( $V_{SS1}$ ) could be measured by another voltage probe between the power source (S) and driver source ( $S_1$ ) as shown in Fig. 2. Then, the bond wire resistance ( $R_{BW}$ ) can be calculated by the voltage across it ( $V_{SS1}$ ) and the SC current ( $I_D$ ) in order to understand whether the SC stress has any impact on the bond wire resistance.

During each SC test, the average bond wire resistance is calculated from  $t = 1 \mu s$  to  $2 \mu s$  and the variation of average bond wire resistance with increasing number of repetitions at different case temperatures are shown in Fig. 11. The bond

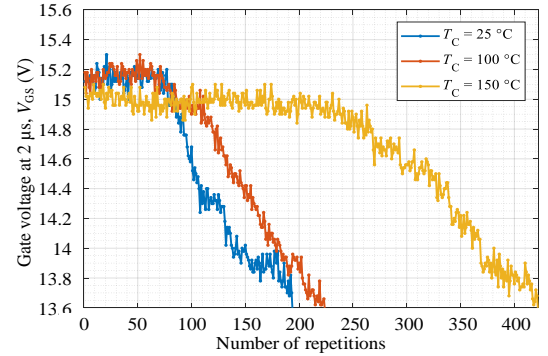


Fig. 7. Gate voltage at 2  $\mu s$  ( $V_{GS}$ ) variation with increasing SC repetitions at different case temperature.

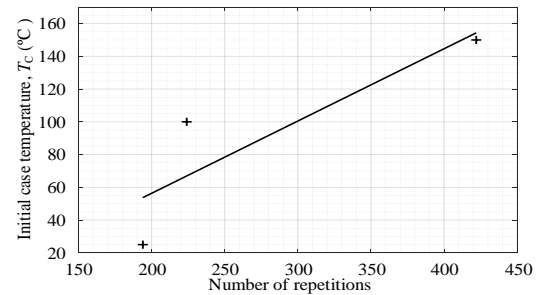


Fig. 8. Correlation between the number of repetitions and the case temperature .



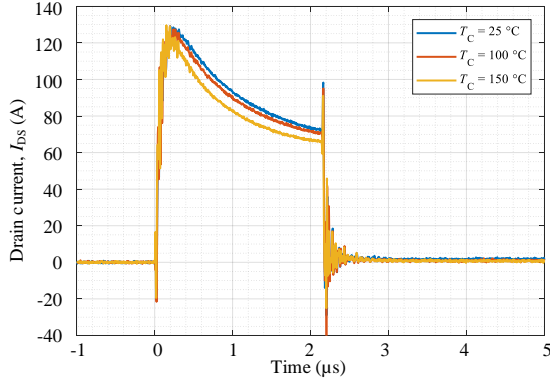


Fig. 9. Drain-source current waveforms during the 1<sup>st</sup> repetition SC test at different case temperatures.

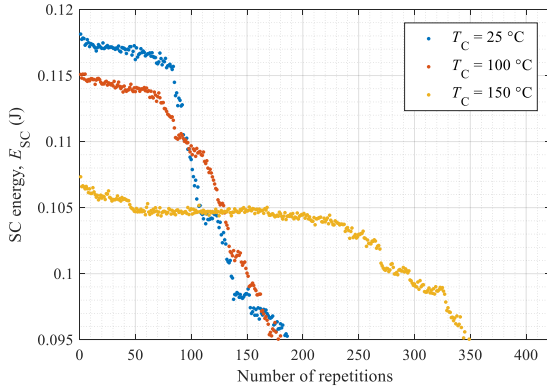


Fig. 10. Short-circuit energy ( $E_{SC}$ ) variation with increasing number of SC repetitions at different case temperatures (25 °C, 100 °C and 150 °C).

wire resistance during repetitive SC tests at 25 °C case temperatures remains relatively constant with increasing number of repetitions and it increases a little at the end of SC repetitions. At the case temperature of 100 °C and 150 °C, the bond wire voltages are also measured in the same way and the bond wire resistance remain constant with the repetitions increase. This means that the SC stress has a negligible effect on the reliability of the bond wire; instead, the SC stress has a major impact on chip-related failures, such as gate failure.

#### IV. CONCLUSIONS

This paper points out an obvious impact of case temperature on the SC behavior for 1000 V /22 A SiC MOSFETs with 3<sup>rd</sup> generation planar technology. At first, the temperature-dependent SC capability is verified by increasing the SC pulse time duration step by step. The maximum SC withstanding time duration is reduced with increasing case temperature. Drain leakage current induced by thermal generation current leads to the thermal runaway after the device turns off.

Thereafter, the test conditions for repetitive SC tests are selected below the critical energy and the static characteristics are measured after 10 SC repetitions. A gate oxide failure is observed with increasing number of repetitions. The correlation between the on-state gate voltage during SC tests and the gate leakage current is confirmed and in this case, a 9.3% reduction of on-state gate voltage is considered as the aging indicator for failure.

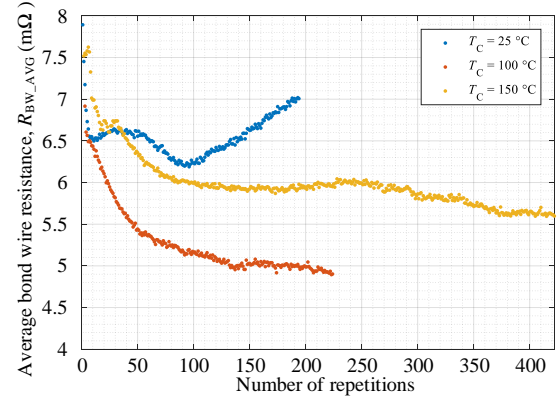


Fig. 11. Average bond wire resistance ( $R_{BW\_AVG}$ ) variation with increasing number of SC repetitions at different case temperatures (25 °C, 100 °C and 150 °C).

The results of repetitive SC tests show that the number of repetitions increases with increasing initial case temperature. This phenomenon could be explained by the lower SC energy due to the drain current reduction at higher case temperatures. The correlation between the case temperature and number of repetitions could be used for lifetime modeling purpose in operating conditions. The bond wire resistance is also observed under repetitive SC tests, which indicates that SC stress has a negligible effect on its reliability.

#### REFERENCES

- [1] M. Nawaz and K. Ilves, "Replacing Si to SiC: Opportunities and challenges," *Eur. Solid-State Device Res. Conf.*, 2016, pp. 472–475.
- [2] K. Hamada *et al.*, "3.3 kV/1500 A power modules for the world's first all-SiC traction inverter," *Jpn. J. Appl. Phys.*, vol. 54, no. 4S, p. 04DP07, Apr. 2015.
- [3] S. Sabri *et al.*, "New generation 6.5 kV SiC power MOSFET," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2017, pp. 246–250.
- [4] D. Grider *et al.*, "10 kV/120 A SiC DMOSFET half H-bridge power modules for 1 MVA solid state power substation," in *2011 IEEE Electric Ship Technologies Symposium*, 2011, pp. 131–134.
- [5] G. Wang *et al.*, "Static and dynamic performance characterization and comparison of 15 kV SiC MOSFET and 15 kV SiC n-IGBTs," in *2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2015, pp. 229–232.
- [6] A. Fayyaz, L. Yang, M. Riccio, A. Castellazzi, and A. Irace, "Single pulse avalanche robustness and repetitive stress ageing of SiC power MOSFETs," *Microelectron. Reliab.*, vol. 54, no. 9–10, pp. 2185–2190, 2014.
- [7] C. Ionita, M. Nawaz, K. Ilves, and F. Iannuzzo, "Short-circuit ruggedness assessment of a 1.2 kV/180 A SiC MOSFET power module," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 1982–1987.
- [8] T. T. Nguyen, A. Ahmed, T. V. Thang, and J. H. Park, "Gate Oxide Reliability Issues of SiCMOSFETs Under Short-Circuit Operation," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2445–2455, 2015.
- [9] L. Ceccarelli, P. D. Reigosa, F. Iannuzzo, and F. Blaabjerg, "A

- survey of SiC power MOSFETs short-circuit robustness and failure mode analysis,” *Microelectron. Reliab.*, vol. 76–77, pp. 272–276, 2017.
- [10] S. Mbarek, P. Dherbécourt, O. Latry, and F. Fouquet, “Short-circuit robustness test and in depth microstructural analysis study of SiC MOSFET,” *Microelectron. Reliab.*, vol. 76–77, pp. 527–531, 2017.
- [11] T. Santini, M. Sebastien, M. Florent, L. V. Phung, and B. Allard, “Gate oxide reliability assessment of a SiC MOSFET for high temperature aeronautic applications,” *2013 IEEE ECCE Asia Downunder - 5th IEEE Annu. Int. Energy Convers. Congr. Exhib. IEEE ECCE Asia 2013*, pp. 385–391, 2013.
- [12] F. Boige, F. Richardeau, D. Trémouilles, S. Lefebvre, and G. Guibaud, “Investigation on damaged planar-oxide of 1200 V SiC power MOSFETs in non-destructive short-circuit operation,” *Microelectron. Reliab.*, vol. 76–77, pp. 500–506, 2017.
- [13] D. Pappis, L. de Menezes, and P. Zacharias, “Comparison of the Short Circuit Capability of Planar and Trench SiC MOSFETs,” in *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2017, pp. 1–9.
- [14] X. Zhou, H. Su, Y. Wang, R. Yue, G. Dai, and J. Li, “Investigations on the Degradation of 1.2-kV 4H-SiC MOSFETs under Repetitive Short-Circuit Tests,” *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4346–4351, 2016.
- [15] Z. Wang *et al.*, “Temperature-Dependent Short-Circuit Capability of Silicon Carbide Power MOSFETs,” *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1555–1566, 2016.